I Claim:

1. An apparatus for converting a differential input signal to a single output signal; said differential input signal including a first signal component and a second signal component; the apparatus comprising:

(a) a first buffer structure receiving said first signal component at a first input locus; said first buffer structure presenting a first buffer output signal representative of said first signal component at a first buffer output locus; said first buffer structure generating at least one first representative signal related to said first signal component;

(b) a second buffer structure receiving said second signal component at a second input locus; said second buffer structure presenting a second buffer output signal representative of said second signal component at a second buffer output locus; said second buffer structure generating at least one second representative signal related to said second signal component;

(c) a control unit coupled with at least one buffer output locus of said first buffer output locus and said second buffer output locus; said control unit comparing said at least one buffer output signal with a reference signal to generate at least one control signal; said at least one control signal affecting at least one signal component of said first signal component and said second signal component to reduce drift of said at least one signal component; and

(d) an output unit coupled for receiving said at least one first representative signal from said first buffer structure and for receiving said at least one second representative signal from said second buffer structure; said output unit combining said at least one first representative signal and said at least one second representative signal to present said single output signal at a signal output locus; said single output signal being related to a sum of said first representative signal and said second representative signal; said single output signal having a variance range limit substantially between said first signal limit and said second signal limit.

2. An apparatus for converting a differential input signal to a single output signal as recited in Claim 1 wherein said first buffer output locus and said second buffer output locus are connected electrically in common.

3. An apparatus for converting a differential input signal to a single output signal as recited in Claim 2 wherein said at least one buffer output signal is said first buffer output signal and said second buffer output signal, and wherein said control unit compares said first buffer output signal and said second buffer output signal with said reference signal.

4. An apparatus for converting a differential input signal to a single output signal as recited in Claim 1 wherein said at least one first representative signal is at least one first current, said at least one second representative signal is at least one second current and said output unit is embodied in a current mirror.

5. An apparatus for converting a differential input signal to a single output signal as recited in Claim 2 wherein said at least one first representative signal is at least one first current, said at least one second representative signal is at least one second current and said output unit is embodied in a current mirror.

6. An apparatus for converting a differential input signal to a single output signal as recited in Claim 3 wherein said at least one first representative signal is at least one first current, said at least one second representative signal is at least one second current and said output unit is embodied in a current mirror.

7. An apparatus for receiving a fully differential input signal and presenting a single-ended output signal representative of said differential input signal; said differential input signal including a plurality of input signal components; the apparatus comprising:

(a) a plurality of input units; each respective input unit of said plurality of input units receiving at least one said respective input signal component of said plurality of input signal components from a respective input signal line of a plurality of input signal lines;

(b) a feedback unit coupled with selected input signal lines of said plurality of input signal lines and coupled with said plurality of input units for receiving a respective treated output signal from each said respective input unit; said feedback unit comparing each said respective treated output signal with a reference signal; said feedback unit generating a respective feedback signal from each said comparing; each said respective feedback signal affecting a respective selected said input signal component to reduce drift of said respective selected input signal component; and

(c) a combining unit; said combining unit being coupled with at least one first selected input unit of said plurality of input units for receiving at least one first representative signal from said at least one first selected input unit; said combining unit being coupled with at least one second selected input unit of said plurality of input units for receiving at least one second representative signal from said at least one second selected input unit; said combining unit generating said single-ended output signal at an output locus; said single-ended output signal being related to said at least one first representative signal from each of said at least one first selected input units and said at least one second representative signal from each of said at least one second selected input units.

8. An apparatus for receiving a fully differential input signal and presenting a single-ended output signal representative of said differential input signal as recited in Claim 7 wherein said selected input signal lines comprise each said respective input signal line.

9. An apparatus for receiving a fully differential input signal and presenting a single-ended output signal representative of said differential input signal as recited in Claim

7 wherein said plurality of input units comprises a first buffer unit and a second buffer unit, wherein said at least one first selected input unit is said first buffer unit and wherein said at least one second selected input unit is said second buffer unit.

10. An apparatus for receiving a fully differential input signal and presenting a single-ended output signal representative of said differential input signal as recited in Claim 7 wherein said at least one first representative signal is at least one first current, said at least one second representative signal is at least one second current and said output unit is embodied in a current mirror.

11. An apparatus for receiving a fully differential input signal and presenting a single-ended output signal representative of said differential input signal as recited in Claim 8 wherein said plurality of input units comprises a first buffer unit and a second buffer unit, wherein said at least one first selected input unit is said first buffer unit and wherein said at least one second selected input unit is said second buffer unit.

12. An apparatus for receiving a fully differential input signal and presenting a single-ended output signal representative of said differential input signal as recited in Claim 8 wherein said at least one first representative signal is at least one first current, said at least one second representative signal is at least one second current and said output unit is embodied in a current mirror.

13. An apparatus for receiving a fully differential input signal and presenting a single-ended output signal representative of said differential input signal as recited in Claim 9 wherein said at least one first representative signal is at least one first current, said at least one second representative signal is at least one second current and said output unit is embodied in a current mirror.

14. A method for converting a differential input signal to a single output signal; said differential input signal including a first signal component and a second signal component; the method comprising the steps of:

(a) in no particular order:

(1) providing a first buffer structure for receiving said first signal component at a first input locus;

(2) providing a second buffer structure receiving said second signal component at a second input locus;

(3) providing a control unit coupled with said first buffer and said second buffer; and

(4) providing an output unit coupled with said first buffer structure and with said second buffer structure;

(b) operating said first buffer structure to present a first buffer output signal representative of said first signal component at a first buffer output locus, and to generate at least one first representative signal related to said first signal component;

(c) operating said second buffer structure to present a second buffer output signal representative of said second signal component at a second buffer output locus, and to generate at least one second representative signal related to said second signal component;

(d) operating said control unit to compare said first buffer output signal and said second buffer output signal with a reference signal to generate at least one control signal;

(e) employing said at least one control signal to affect said first signal component and said second signal component to reduce drift of said first signal component and said second signal component; and

(f) operating said output unit to combine said at least one first representative signal and said at least one second representative signal to present said single output signal at a signal output locus; said single output signal being related to a sum of said at least one first representative signal and said at least one second

representative signal; said single output signal having a variance range limit substantially between said first signal limit and said second signal limit.

15. A method for converting a differential input signal to a single output signal as recited in Claim 14 wherein said at least one first representative signal is at least one first current, said at least one second representative signal is at least one second current and said output unit is embodied in a current mirror.